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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/089,666	06/03/98	YAMAMOTO Y	149733/97

MM42/0921

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EXAMINER	
HACK, J	
ART UNIT	PAPER NUMBER
2812	5

DATE MAILED: 09/21/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/089,666	Applicant(s) Yamamoto
	Examiner Jonathan Hack	Group Art Unit 2812

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-20* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-20* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 3

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: page 11, line 20 refers to Figure 8, however, Figure 8 is not provided.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al US Patent 5,707,896 in view of Wolf, Silicon Processing for the VLSI Era Vol. 2 pages 144-147 (1990).

Chaing et al discloses the invention of claims 1, 7, 8, 10 and 15-16 as follows:

forming a field oxide film on a semiconductor substrate to form an element isolation region (see Figure 2, item 12);

forming a side wall film formed of an insulation material on a side wall of a gate electrode which is formed on said semiconductor substrate (see Figure 2, item 26 and column 5, lines 13-14);

injecting ion injection species into said semiconductor substrate using said gate electrode as a mask, thereby forming a diffusion layer (see Figure 3, items 32 and column 5, lines 22-39);

activating said diffusion layer by a first thermal treatment (see column 6, lines 20-23);

depositing titanium on the entire surface of said semiconductor substrate and performing a second thermal treatment, thereby forming a Ti silicide either on said gate electrode or on said diffusion layer in a self-aligned manner (see column 5, lines 63-66)

wherein a third thermal treatment at a temperature lower than that of the first thermal treatment for the activation is carried out between the ion injection for forming said diffusion layer and the first thermal treatment for activating said diffusion layer, thereby discharging fluorine produced from the ion injection species to the outside from a surface of said field oxide film, a surface of said side wall film, said semiconductor substrate, and an interface between said semiconductor substrate and said field oxide film (see column 5, lines 48-62).

Chaing et al makes mention of a metal wiring layer, but does not detail a metal layer deposited, reacted and unreacted metal removed as stated by the instant invention. However, this technique is fully described in Wolf (see page 144-147).

In addition, Chaing et al does not explicitly state that there is an activation of the ions to form the diffusion layer. However, Chaing et al does describe additional heating steps which will

activate the dopants. Further, activating dopants is common in semiconductor fabrication to complete the source/drain regions.

For claim 2,

wherein said third thermal treatment is consecutively performed in the same apparatus as that of said first thermal treatment for activating said diffusion layer (see column 5, line 56 through column 23).

For claims 3 and 8,

wherein said ion injection species injected into said diffusion layer are ions including fluorine and boron (see column 5, lines 35-39).

For claims 4 and 9, Chaing et al does not explicitly state,

wherein a fluorine concentration is set to be 1 E20 atoms/cm^3 or less by said third thermal treatment.

However, the ion implantation and thermal treatment of the instant invention and the ion implantation and the thermal treatment of Chaing et al are conducted in similar ion doses and similar ranges of time and temperature and all performed in similar stages of the process (see column 5, lines 33-62). As a result of these similar steps, it would be an inherent feature of Chaing et al that the fluorine concentration of Chaing et al would be similar to the fluorine concentration of the instant invention after the third thermal treatment.

For claim 5,

wherein a temperature of said third thermal treatment is at a range of 300 to 750 °C (see column 5, lines 56-62).

For claim 6, official notice is taken for the limitation of,

wherein an apparatus for carrying out said third treatment is a diffusion furnace, a RTP apparatus and a hot plate,

is a common feature for diffusion in semiconductor processing.

4. Claims 11-14, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaing et al US Patent 5,434,096 in view of Wolf, Silicon Processing for the VLSI Era Vol. 2 pages 144-147 (1990) as applied to claim 7 above, and further in view of Kitano US Patent 5,665,646.

Chaing et al and Wolf are applied supra and Kitano discloses the added limitations for claims 11 and 17,

wherein said silicide has C49 phase (see column 4, lines 5-16).

For claims 12 and 18,

changing a phase of said silicide from C49 to C54 (see column 4, lines 17-27).

For claims 13 and 19, see the rejection of claim 3.

For claims 14 and 20, see the rejection of claim 9.

Given the disclosure of Kitano, it would have been obvious to one of ordinary skill in the art at the time the invention was made to change the silicide from C49 phase to C54 phase because C54 has a low resistance.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan Hack whose telephone number is (703) 308-1341. The examiner can normally be reached on Monday to Friday from 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached on (703) 308-3325. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jonathan Hack
Art Unit 2812
September 15, 1999

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800